PCI Express®
Protocol Solutions for Testing and Compliance

TELEDYNE LECROY
Everywhereyoulook™

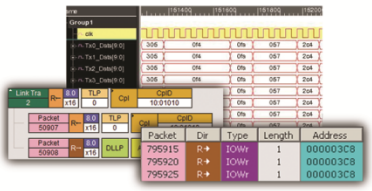
Summit™ T3-16 Analyzer
Summit Z3-16 Exerciser
Summit T3-8 Analyzer
Summit T34 Analyzer
Summit T28 Analyzer
Summit T24 Analyzer
PCIe® 3.0 Compliance Testing

COMPLETE PROTOCOL TEST SOLUTIONS

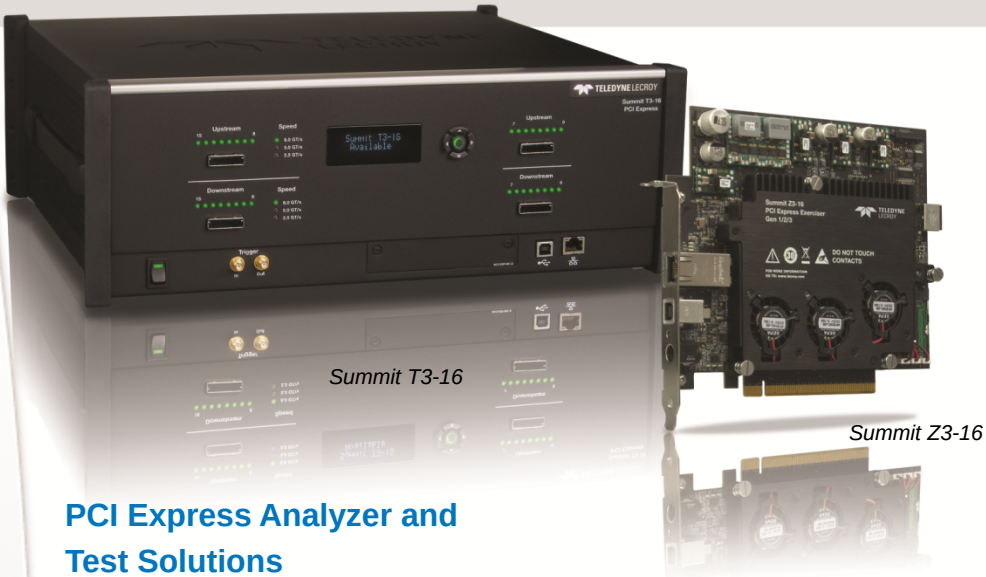
Teledyne LeCroy, a worldwide leader in serial data test solutions, creates advanced instruments that drive product innovation by quickly measuring, analyzing, and verifying complex electronic signals. With systems available for both physical and protocol layer testing, Teledyne LeCroy offers compre-hensive solutions to meet the high demands of PCI Express devices and software.

Our commitment and leadership in protocol test for PCI Express has been clearly demonstra-ted with our impressive list of "industry firsts", which include the first Gen1 x16 analyzer, the first Gen2 x16 analyzer and both the first Gen3 x16 analyzer & exerciser.

SimPASS™ PE



Analyze RTL vector files with the power of a protocol analyzer!



Summit T3-16

Summit Z3-16

PCI Express Analyzer and Test Solutions

The Teledyne LeCroy PCI Express analysis and test systems provide users with accurate, reliable and scalable tools to help with perform-ance measurements and real time monitoring for development and test.

With a wide range of hardware platforms, field upgradeable firmware for protocol updates, and the industry's largest assortment of probes and interposers, these systems can evolve as your protocol analysis needs change. The PCI Express solutions include protocol analyzers and exercisers, and support lane widths from single lane to x16 and data rates of 2.5 GT/s to 8 GT/s.

Analyzers for Every Speed and Lane Width

Analyzer solutions start from the low cost portable Summit T24 to the advanced Summit T3-16 analyzer, Teledyne LeCroy's fifth generation analyzer, which includes the latest in PCIe 3.0 analysis features.

An Exerciser for Every Need

The PCI Express Z3-16 exerciser assists with generating PCI Express transactions, observing behavior, and performing both stress testing and compliance testing. It provides extensive root complex or end point emulation capabilities.

As complete solutions, the Summit analyzer and Summit exerciser products give you the unique ability to record (capture) live traffic, modify the traffic, and then playback the transactions in "script" form, using the exerciser.

Connectivity— Probes and Interposers

Without the right connectivity to your application even the most powerful analyzer is rendered ineffective. Teledyne LeCroy analyzers have the largest assortment of PCI Express probes and interposers of any analyzer vendor. The interposer probes give you high-fidelity, non-

ANALYZERS	Summit T3-16	Summit T3-8	Summit T34	Summit T28	Summit T24
Speed	Up to 8 GT/s	Up to 8 GT/s	Up to 8 GT/s	Up to 5 GT/s	Up to 5 GT/s
Lanes	x1 to x16	x1 to x8	x1 to x4	x1 to x8	x1 to x4

T.A.P. 3 Transparent Acquisition Probing Technology

intrusive taps to capture the signals between a system board and an add-in card. MidBus and multi-lead probes allow you to capture inter-chip signaling within a PCI Express board, through either a header connection or a probe tip.

Powerful Display Views Allow for Easy Analysis of Protocol Traffic

Teledyne LeCroy's analysis software gives you a variety of powerful tools for analyzing and displaying traffic. The software makes it easy for you to view all elements of a transaction, even if they are spread over several different physical links—helping you understand traffic flow and ensure devices are behaving correctly at the protocol level

Unfiltered PCI Express traffic contains tens of thousands of packets, which can make it extremely difficult for you to discover and analyze errors within the data. Within the CATC Trace™ software display, you can preserve the detail, but also have an easy way to view the traffic hierarchically.

For instance, you can:

- Push a button and get a listing of all protocol errors in a trace. All errors are hyperlinked to the trace for further analysis.
- Change protocol views with the push of a button to examine data link layer packets and transaction layer packets to verify correct ACK/NAK and completion TLP handshaking. Packets are shown with pertinent information such as packet number, direction of flow, header, flow control status, time stamp, data, ACK/NAK, and other packet level information.
- With another button, quickly decode down to the packet layer to show detailed information of the devices involved, device IDs, types of commands, and performance data.

The Summit Z3-16 Exerciser acts as its own target emulator, and supports host emulation through an optional test platform.

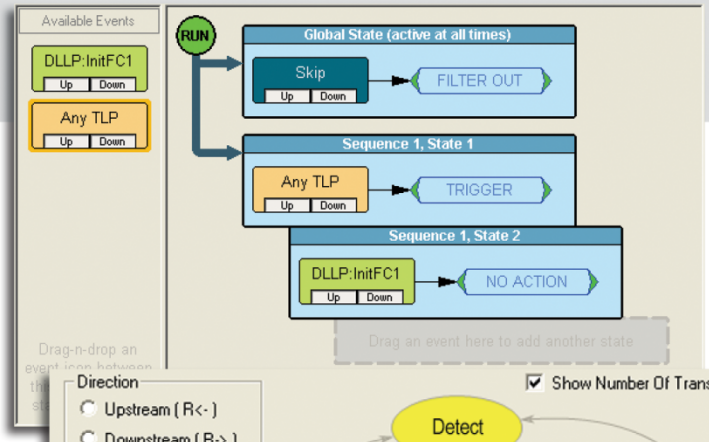
EXERCISER	Summit Z3-16
Speed	Up to 8 GT/s
Lanes	x1 to x16
Scratchpad Script Memory (Device Emul.)	1 GB
Emulation	Host & Device

PROBES	Max Speed	Lanes
Active Interposer	8 GT/s	x1-x16
Passive Interposer	5 GT/s	x1-x16
MidBus Full- and Half-Size Module	8 GT/s	x1-x16
Multi-lead (solder down)	8 GT/s	x1-x16
AMC	5 GT/s	x1-x8
XMC	5 GT/s	x1-x8
ExpressCard	5 GT/s	x1
ExpressModule	8 GT/s	x1-x8
HP BladeSystem Module	5 GT/s	x1-x8
MiniCard	5 GT/s	x1
VPX	5 GT/s	x1-x16
CompactPCI Serial	5 GT/s	x1-x8
External Cable Interposer	5 GT/s	x1-x8
SFF-8639 (single and dual port)	8 GT/s	x1-x4
90 Degree Server Interposer	8 GT/s	x1-x16
M.2	8GT/s	x1-x4

Teledyne LeCroy is an active member of major standards and industry groups committed to the success of the PCI Express Standard

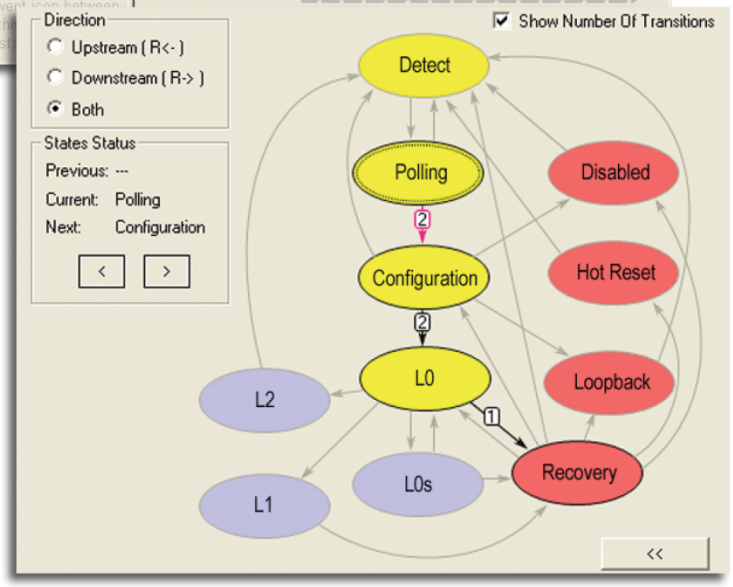
TeleScan PE

TeleScan PE is a configuration space scanning and editing application, supporting all PCIe specifications up to PCIe 3.0. TeleScan PE provides system scan, read, write and decode features for all PCI Express designs. The application shows PCIe bus information in a tree-structured format, including specification descriptions for every field. TeleScan PE is supplied free of charge for all Teledyne LeCroy customers.



Although the CATC Trace display is ideal for showing traffic at the logical level, it is often necessary to drill down to the byte level and see traffic across multiple lanes on a common timescale. The software allows you to easily see the low level primitives and data structures.

Multiple data display formats allow you to see into every aspect of the data traffic, including trace views and LTSSM state views, complete with tool tips to explain details of each field and the ability to "drill down" through protocol layers to track errors to their source.



LTSSM View

Transaction Layer View

Link Layer View

Data Flow View

Special flow control information to allow you to track flow control

Chronological View

Packets grouped and shown in logical order

Automatically decodes TLP, DLLP's, and primitive packets

Indicates data rate (Gen1, Gen2 or Gen3)

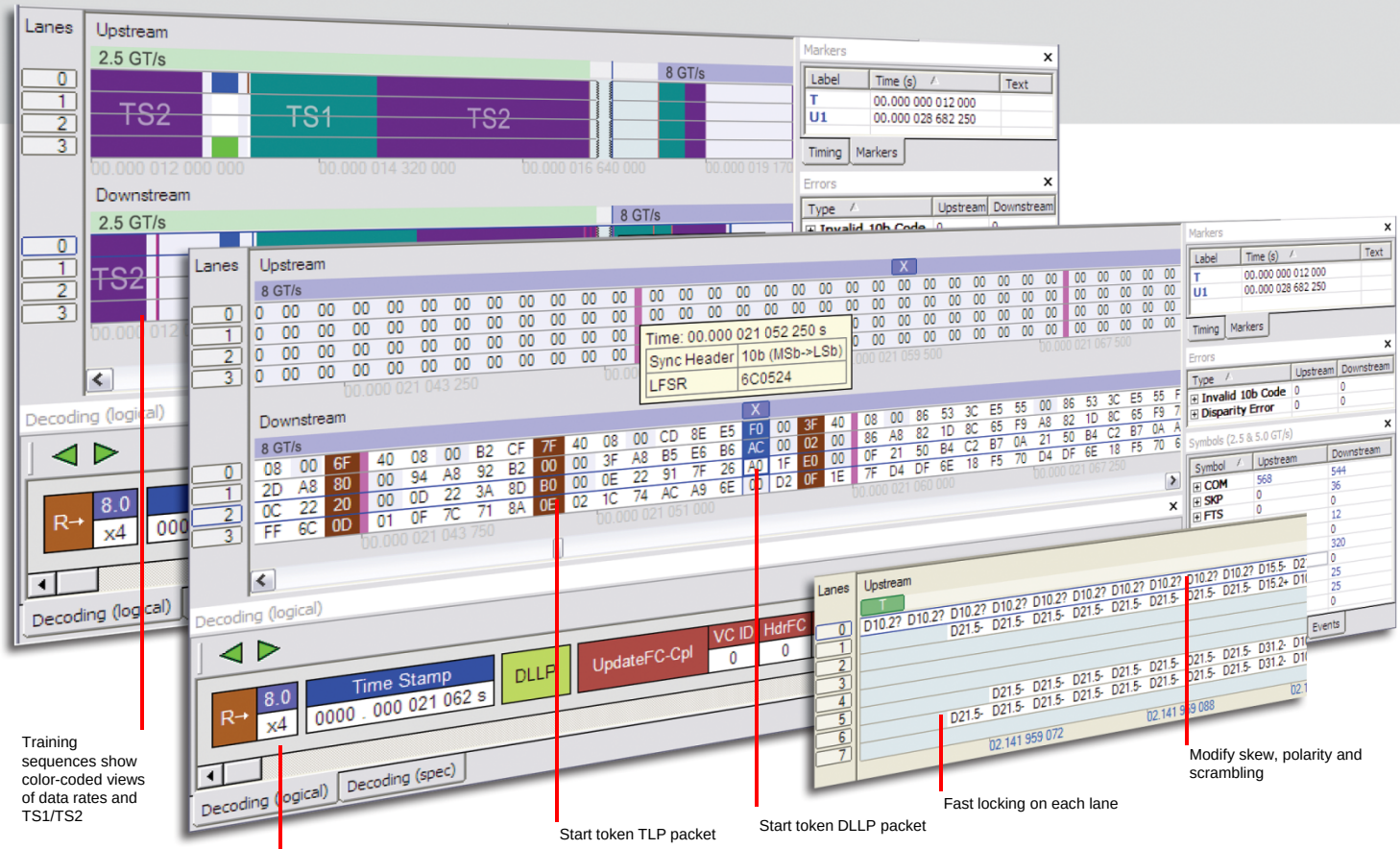
Shows traffic direction

The intuitive CATC Trace™ decodes and displays PCI Express packets with color-coded fields

Link Tracker View

View by direction

Displays protocol errors



BitTracer™ Logic Analyzer Views

Powerful Triggering and Filtering

As the debugging process evolves and moves from prototypes to system level testing, triggering becomes more important since problems from linking devices are increasingly intermittent. The software provides the ability to select simple triggers on typical events, such as errors, link conditions, TLP headers, DLLP packets or payload data. Triggers can be set up on almost any sequence of events possible; it supports up to 32 levels or sequential states. It also allows you to isolate the important part of the traffic stream, and when you open the trace, it jumps right to that portion.

Comprehensive Traffic Reports and Summaries

Our PCI Express solutions are more than just data recorders. The real value is in the analysis of the data. The software presents real time statistics, including link utilization, data payload throughput, and data packet count. It also generates detailed reports that provide statistics on the occurrence of errors and packets, and counts events for the link transactions and split transactions in the trace. You can evaluate these metrics at a glance or use them to navigate through the recording. The traffic summary can be printed or saved to text with a single keystroke

Search Results Quickly

The advanced search features in the software help you quickly find what you want. By using the ZeroTime™ Search, you can select fields right from the drop down menu, such as Go To Trigger or Event, or directly to a specific marker or time stamp in the trace. The Go To feature provides a simple way to search for PCI Express specific items within the trace, such as packets or specific link transactions. The advanced Find lets you search on specific PCI Express parameters such as the TLP Type—Memory Write (32-bit). Using the Find dialog, you can choose your selection criteria and isolate the data you seek.

BitTracer Logic Display

The BitTracer option provides a physical layer traffic view, similar to a logic analyzer, combining the advantages of a protocol analyzer with those of a logic analyzer.

EXERCISERS AND COMPLIANCE TESTING

Advanced Exerciser for PCI Express Traffic Generation

Teledyne LeCroy's Summit Z3-16 exerciser is capable of generating and responding to all types of PCI Express transactions, including both host and device emulation. The powerful scripting language allows for the creation of TLPs and DLLPs. ACK's and NAK's can be automatically generated under your control, or inject CRC errors, and violate flow control credits and other types of errors. You can create test scripts by exporting traffic from a trace file captured with a Summit analyzer. The exported script can then be modified to generate different test cases, insert errors or create loop tests. The point and click capability of the script editor makes modifying or creating scripts from scratch simple. The powerful scripting language allows for a link training script to be created with just three simple commands.

PCIe 3.0 Compliance Testing

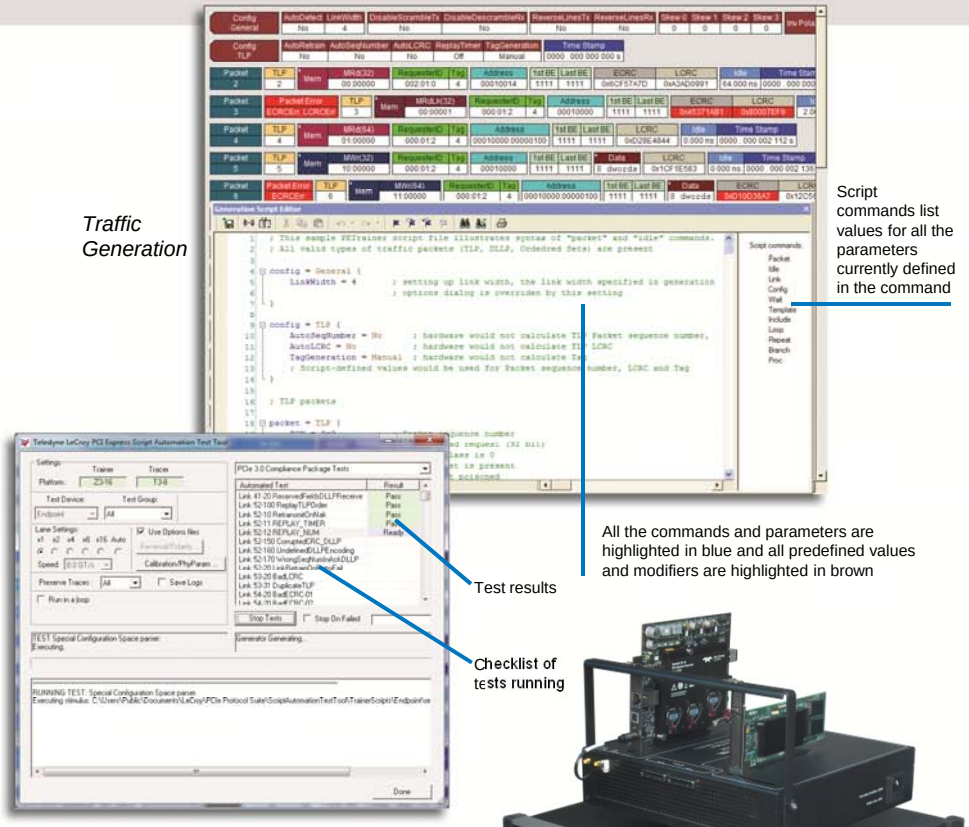
Teledyne LeCroy offers an integrated and automated compliance testing system, including the Protocol Test Card Platform, approved by the PCI-SIG® as a standard tool for compliance testing for developers working with the PCIe 3.0 specification.

NVMe Conformance Testing

Developers of SSDs that utilize SCSI Express, SATA Express or NVMe face challenging testing, problem identification and resolution issues that must be solved quickly to maintain project schedules. Summit analyzers understand and decode these specifications, in addition to all standard PCIe traffic.

In addition, Teledyne LeCroy joined forces with the University of New Hampshire Interoperability Lab (UNH-IOL) to create test procedures that have been accepted as standard NVMe test tools by the PCI-SIG. These test suites, run on Summit analyzers & exercisers, help validate conformance to the requirements of the NVMe specification.

University of New Hampshire InterOperability Laboratory



PCIe 3.0 Compliance Testing

Protocol Test Card (full system shown): *Selected by the PCI-SIG as an official test tool for PCI Express 3.0 and as a standard conformance test tool for NVMe*

A Comprehensive Solution

Teledyne LeCroy's PCI Express solutions provide you with advanced features necessary to ease the development and deployment of PCI Express devices and software. At every level, you have the ability to drill deeper into the data, to get additional information about the traffic or even the protocol itself.

Let Teledyne LeCroy's Serial Data Solutions peel back the layers of PCI Express to solve your test and verification challenges.

Summit Product Family

Host Machine Requirements: Microsoft Windows® 8, Windows Server 2012, Windows 7, Windows Server 2008R2, Windows XP; 2 GB of RAM; Storage with at least 600 MB for the installation of the software and additional space for recorded data; display with resolution of at least 1024x768 with at least 16-bit color depth; and USB 2.0 port and/or 100/1000baseT Ethernet. For optimal performance, please refer to our recommended configuration in the product documentation.

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	Summit T3-16 Analyzer	Summit Z3-16 Exerciser	Summit T3-8 Analyzer	Summit T34 Analyzer	Summit T28 Analyzer	Summit T24 Analyzer
Recording Memory Size	8 GB for trace capture, timing and control information	1 GB trace generation, 1 GB device memory emulation	4 GB for trace capture, timing and control information	4 GB for trace capture, timing and control information	4 GB for trace capture, timing and control information	2 GB for trace capture, timing and control information
Rear Panel Connectors (PCB Connectors for Summit Z3-16)	AC Power, Expansion card slot	12V DC power, x16 PCIe® edge connector, Ext. trigger IN/OUT, Ethernet, USB 2.0 “B” connector	AC Power, x16 expansion port (for second T3-8 system), Sync IN & OUT, Expansion Card Port	12V DC Power, Sync/Data Port, USB 3.0 “B” connector, Ethernet, Port for Expansion to x8 with second T34	12V DC Power, Trigger IN/OUT, Sync IN/OUT, USB 2.0 “B” connector	12V DC Power, Sync IN/OUT, USB 2.0 “B” connector
Front Panel Connectors	Four iPass connectors, Trigger IN/OUT, USB 2.0, Ethernet		Two iPass connectors, Trigger IN/OUT, USB 2.0, Ethernet	iPass x4 connector, Ref Clk IN/OUT, Trigger IN/OUT	Two iPass connectors, Ref Clock IN/OUT	iPass x4 connector
Front Panel Indicators (PCB LEDs for Summit Z3-16)	1” x 3” Display, Record, Trigger and Status LEDs	32 status LEDs (TX/RX for each channel), 4 data rate LEDs	1” x 3” Display, Lane Activity and Data Rate LEDs	8 Lane Activity LEDs; 6 Link Speed LEDs; Power, Status and Trigger LEDs	16 Lane Activity LEDs, Link Speed, Power and Status LEDs	8 Lane Activity LEDs, Link Speed, Power and Status LEDs
Front Panel Controls	Power ON/OFF, Menu Navigation Buttons, Manual Trigger		Power ON/OFF, Menu Navigation Buttons			
Dimensions	15.5” x 14.3” x 5.4” (392x363x137 mm)	6.6” x 5.25” (168 x 133 mm)	15.5” x 14.5” x 3.5” (395x367x89 mm)	8.3” x 11.9” x 1.6” (209x302x40 mm)	10.9” x 7.7” x 2.0” (277x196x51 mm)	6.2” x 9.0” x 1.7” (158x228x44 mm)
Weight	17 lbs (7.7 Kg)	0.9 lbs (0.4 Kg)	13 lbs (5.9 Kg)	3.0 lbs (1.4 Kg)	2.65 lbs (1.2 Kg)	1.68 lbs (0.76 Kg)
Power Requirements	100-240 VAC, 47-63 Hz (universal input), 480 W maximum	12V DC from adapter	100-240 VAC, 50-60 Hz, 230 W max	12V DC from adapter	12V DC from adapter	12V DC from adapter

Environmental Specifications

Common to All Systems

Temperature: Operating	32 °F to 122 °F (0 °C to 50°C)
Temperature: Non-Operating	14 °F to 176 °F (-10 °C to 80 °C)
Humidity: Operating	10% to 90% RH (non-condensing)

FEATURES	BENEFITS
Powerful and Intuitive CATC Trace	Faster interpretation and debug of PCI Express Traffic.
Extensive Decoding	Understand the protocol with accurate, decoding of TLPs (Transaction Layer Packets), DLLPs (Data Link Layer Packets), and all Primitives. Includes extensive decoding of Solid-State Device (SSD) protocols, including NVM Express, SCSI Express and SATA Express.
Advanced Triggering/Filtering	Find errors fast by isolating important traffic, specific errors, or data patterns. Understand transactions by removing non-essential fields from the trace.
Intelligent Reporting	Quickly identify and track error rates, abnormal link or timing conditions, display configuration space, and protocol specification details.
Dword to Transaction Level Viewer	See and understand Symbol, Packet, Link, and Split Transaction protocol levels.
Monitoring and Link Utilization	Troubleshoot throughput, link utilization, and bandwidth issues.
I/O Virtualization	Decode multi-root TLP/DLLPs and single-root configuration space to verify PCI Express functionality and operation.
LTSSM View	View and navigate link states through an abstracted state diagram interface.
Flow Control View	View flow control credits between devices to verify proper performance.
Protocol Test Card Option	Prepare for passing the official PCI-SIG® protocol compliance test.
BitTracer™ Option	Records the bytes as they come across the link. Allows debugging of PHY layer problems. Gives protocol analyzer both a logic analyzer format and decoded protocol analyzer format.
Auto Sense Link	Analyzes all traffic negotiation between two devices of different lane widths.
Lane Swizzling	Accommodates unique board layouts for mid-bus probe pads. In addition, the Summit T3-16, Summit T3-8 and Summit T28 support autoswizzle.
Deep Buffer Recording Capability	Capture long recording sessions for analysis.
T.A.P.^{3} (Transparent Acquisition Probing Technology)	Insures accurate data acquisition at data rates up to 8 GT/s for lane widths from x1 to x16.
High Speed USB Port	No complicated setup required.
Downloadable Trace Viewer	Share and annotate trace recordings within a team.

ProtoSync PE

View Gen3 protocol precursor, cursor and post-cursor coefficients. Then see how they affect electrical characteristics of the signal.

ORDERING INFORMATION

Product Description	Product Code
Summit T3-16 Analyzer	
Summit T3-16 Gen3 x16 Analyzer	PE050AAA-X
Summit T3-16 Gen3 x8 Analyzer	PE051AAA-X
Summit T3-8 Analyzer	
Summit T3-8 Gen3 x8 Analyzer	PE060AAA-X
Summit T3-8 Gen3 x4 Analyzer	PE061AAA-X
Summit T34 Analyzer	
Summit T34 Gen3 x4 Analyzer	PE080AAA-X
Summit T28 Analyzer	
Summit T28 Gen2 x8 Analyzer	PE070AAA-X
Summit T28 Gen2 x4 Analyzer	PE071AAA-X
Summit T24 Analyzer	
Summit T24 Gen2 x4 Analyzer	PE076AAA-X

Product Description	Product Code
Protocol Test Card	
PCIe 3.0 Protocol Test Card	PE069ABA-X
Summit Z3-16 Exerciser	
Summit Z3-16 Gen3 x16 Exerciser (Device Emulation)	PE050AGA-X
Summit Z3-16 Gen3 x16 Test Platform (used for host emulation)	PE050UEA-X
Interposers and Probes (see probe datasheet for a complete list)	
Gen3 x16 Active Interposer	PE043UIA-X
Gen3 x8 Active Interposer	PE044UIA-X
Gen3 x8 Right 90 Degree Server Interposer	PE058UIA-X
Gen3 x8 MidBus Probe Kit (two kits required for x16)	PE050ACA-X
Gen2 x16 Active Interposer	PE018UIA-X
Gen2 x16 Passive Interposer	PE075UIA-X
Gen3 x16 Multi-lead Probe Pod	PE066UIA-X

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Local sales offices are located throughout the world.
Visit our website to find the most convenient location.

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